**UNITED STATES DEPARTMENT OF COMMERCE**
**Patent and Trademark Office**
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

RD

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. |
|---|---|---|---|
| 09/428,052 | 10/27/99 | IRINO K | 970901A |

MM92/0126

ARMSTRONG WESTERMAN HATTORI
MCLELAND & NAUGHTON
SUITE 1000
1725 K STREET NW
WASHINGTON DC 20006

| EXAMINER | |
|---|---|
| DIAZ,J | |
| **ART UNIT** | **PAPER NUMBER** |
| 2815 | |

**DATE MAILED:** 01/26/01

**Please find below and/or attached an Office communication concerning this application or proceeding.**

**Commissioner of Patents and Trademarks**

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/428,052 | IRINO, KIYOSHI | |
| | Examiner | Art Unit | |
| | José R. Díaz | 2815 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *27 December 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *6 and 8-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6 and 8-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. § 119**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

**Attachment(s)**

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

➢ The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

➢ Claims 6, 9, and 13 rejected under 35 U.S.C. 102(e) as being anticipated by Ito et al. (US Patent No. 5,808,348).

Regarding claim 6, Ito et al. teach a method of fabricating a semiconductor device comprising the steps of: forming a gate oxide film (12) on a substrate (10); forming a gate electrode pattern (20) on said gate oxide film (12); and introducing N atoms into said gate oxide film (12) while using said gate electrode pattern (20) as a mask (column 3, lines 25-27, 30-35, and 40-43), wherein said step of introducing N atoms into said gate oxide film comprises a thermal annealing process of said gate oxide film conducted in an atmosphere containing N atoms and O atoms (column 5, lines 65-66).

Regarding claim 9, Ito et al. teach that said atmosphere contains $N_2O$ (column 5, lines 65-66) and said thermal annealing process is conducted at a temperature of about 900 °C (column 3, lines 38-39).

Regarding claim 13, Ito et al. teach forming diffusion regions (28, 30) at both lateral sides of said gate electrode pattern (20) by introducing impurity elements into

said substrate (10) through said gate oxide film (12) while using said gate electrode pattern (20) as a mask, and wherein said step of introducing impurity elements is conducted prior to said step of introducing N atoms into said gate oxide film (12) (column 4, lines 34-39).

➢ Claims 10-12 rejected under 35 U.S.C. 102(e) as being anticipated by Arai et al. (US Patent No. 972,783).

Regarding claim 10, Arai et al. teach a method of fabricating a semiconductor device comprising the steps of: forming a gate oxide film (2) on a substrate (1); forming a gate electrode pattern (3) on said gate oxide film (2); and introducing N atoms into said gate oxide film (2) while using said gate electrode pattern (3) as a mask, wherein said step of introducing N atoms into said gate oxide film includes an ion implantation process of N ions (column 12, lines 37-39, 44-49 and 55-56).

Regarding claim 11, Arai et al. teach an acceleration voltage of about 10 keV (column 12, lines 69).

Regarding claim 12, Arai et al. teach a dose of about 1-3 x $10^{14}$ $cm^{-2}$ (column 12, lines 61-62).

***Claim Rejections - 35 USC § 103***

➢ The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

➢ Claim 8 rejected under 35 U.S.C. 103(a) as being unpatentable over Ito et al. (US Patent No. 5,808,348) in view of Maiti et al. ("Oxynitride gate dielectric grown in nitric oxide (NO): the effect of reoxidation on dielectric reliability of the active edge", IEEE Electron Device Letters, Volume: 17 Issue: 6 , June 1996 Page(s): 279 -281).

Ito et al., as stated supra, essentially discloses the claimed invention but fails to show the steps of annealing said gate oxide film in an atmosphere containing NO at about 800 °C. Regarding claim 8, Maiti et al. teach that it is well known in the art to anneal in a NO ambient at 850 °C to reduces local build-up of positive charge near the gate electrode (See Section II: Experimental).

Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to have modified Ito et al. to include annealing the gate oxide in a NO ambient at 850 °C as taught by Maiti et al. since such modification would result in a reduction of the local build-up of positive charge near the gate electrode, as described in Abstract of Maiti et al.

***Response to Amendment***

➢ Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

***Conclusion***

➢ The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Wu (US Patent No. 5,880,508) discloses MOSFET with a High Permitivity gate dielectric. Sun et al. (US Patent No. 5,880,040) disclose gate dielectric based on oxynitride grown in $N_2O$ and annealed in NO. Wang et al. (US Patent No.

5,747,882) disclose device including means for preventing tungsten silicide. Loh et al. (US Patent No. 5,516,707) disclose large-tilted angle N implant into dielectric regions overlying source/drain regions of a transistor. Gardner et al. (US Patent No. 5,783,469) disclose method of making nitrogenated gate structure. Min et al (IEE) disclose impact of process-induced damage by the use of NO-base oxynitride gate dielectric. Bhat et al. (IEE) disclose performance and hot-carrier reliability of N- and P- MOSFETs with RTA NO-nitrided $SiO_2$ gate dielectrics.

***Correspondence***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (703) 308-6078. The examiner can normally be reached on 8:00 - 5:00 Monday through Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JRD
January 10, 2001

EDDIE C. LEE
PRIMARY EXAMINER